ABSTRACT

A semiconductor chip comprises a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other. A bond pad-wiring pattern is formed on the semiconductor substrate. A pad-rearrangement pattern is electrically connected to the bond pad-wiring pattern. The pad-rearrangement pattern includes a bond pad disposed over at least a part of the cell region. The bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate. Thus, with the embodiments of the present invention, the overall chip size can thereby be substantially reduced and an MCP can be fabricated without the problems mentioned above.